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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2024**

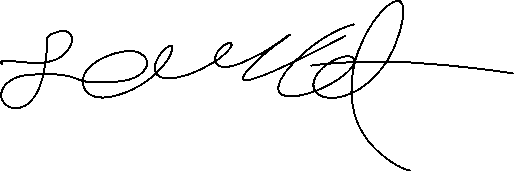
**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Logan Current**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Date: 11/6/2024**



**Report due date: 11/6/2024**

1. **OBJECTIVE**

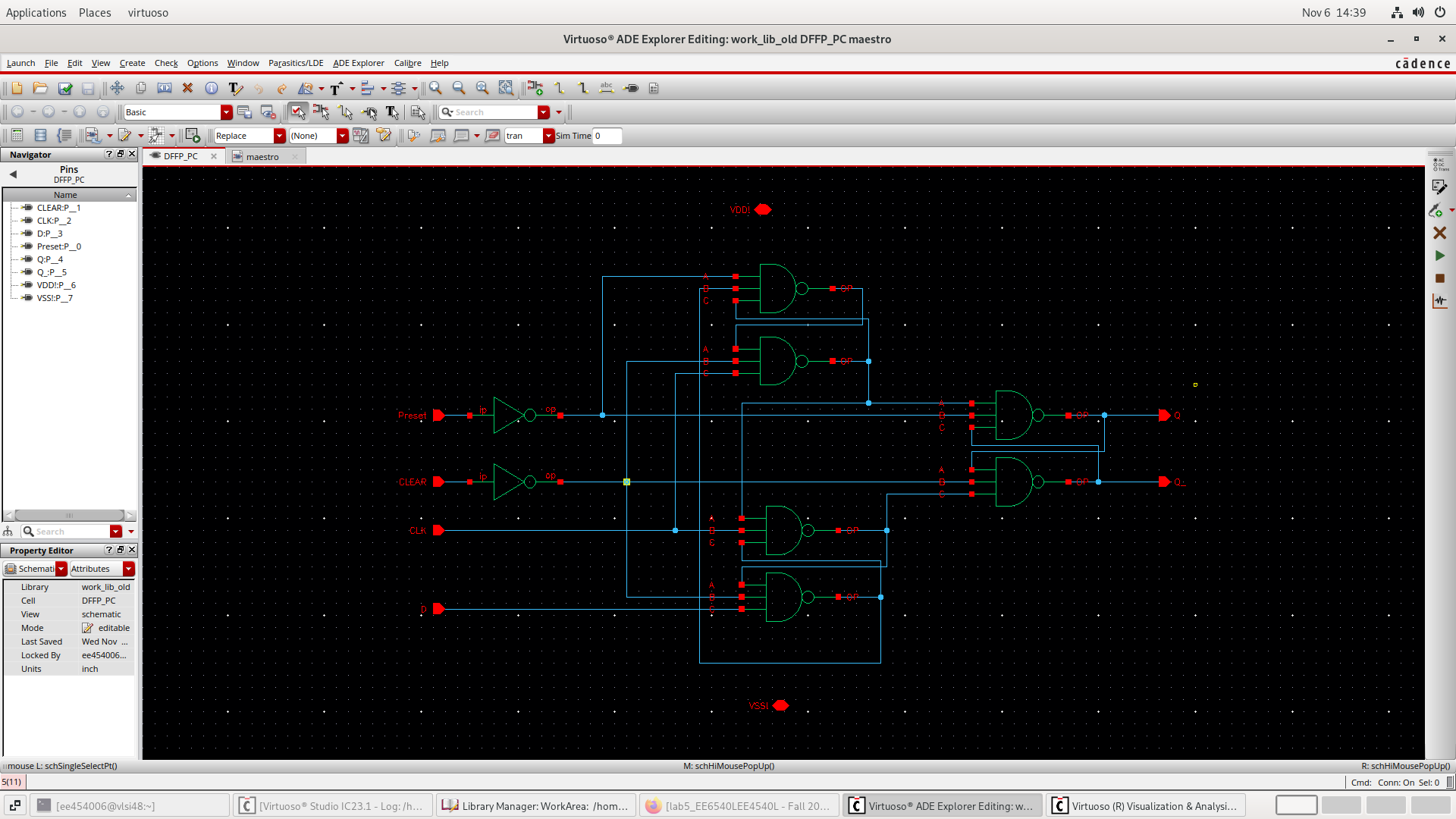
The Objective of this lab is to optimize our NAND3 transistor sizes and use it to make a D-Type Flip Flop with preset as well as clear.

1. **PROCEDURE**

First, I optimized my transistor sizes for my NAND3 to get a better overall propagation delay. With this, I made the D-type Flip Flop (DFF) that included an asynchronous preset and clear. Then, I made the stimuli and generated the waveform to test my design. After, I made the right design, I labeled the graph and found the rising and falling propagation delay.

1. **RESULT**

The order for the screenshots is the transistor level schematic and the waveform,

DFF:A computer screen shot of a black screen

Description automatically generated

1. **CONCLUSION**

This lab wasn’t bad for me. The longest part was getting my final DFF design to work and output the right output.